



OCXO: PT626 - 13 - PLL

- 1MHz to 1GHz PLL hybrid OCXO module phase locked to external 10.00MHz precision reference
- sine wave output, 0dBm into 50Ω
- Hermetically sealed case, 13mm height
- h.f. Communications equipment, system synchronisation, precision reference



Generic specification:

Stability:

OCXO holdover from $\pm 0.005\text{ppm}(0 +50)^\circ\text{C}$, custom specified
 locked dependent upon input reference accuracy
 input reference 10.000MHz, 0dBm, as standard, +2dBm $\pm 6\text{dB}$
 against V_{cc} change $\pm 0.002\text{ppm max.}$, $V_{cc} \pm 5\%$
 against load change $\pm 0.0002\text{ppm max.}$, load $\pm 10\%$
 ageing short term $\pm 0.0003\text{ppm max./day}$ after 30 days continuous operation
 ageing long term from $\pm 0.1\text{ppm max./year}$ after 30 days continuous operation
 electronic trim $\pm 1.0\text{ppm min.}$, no reference

Output:

sine wave, +0dBm min.
 harmonics -25dBc

Power supplies:

supply voltage +5Vd.c. $\pm 5\%$
 start up current 560mA max.
 quiescent current 270mA max. at +25°C
 warm up time 4 minutes max. to within $\pm 0.1\text{ppm}$ of nominal

Typical 10MHz free run phase noise:

single sideband, -130dBc/Hz, $f_o + 10\text{Hz}$
 1Hz bandwidth -150dBc/Hz, $f_o + 100\text{Hz}$
 -160dBc/Hz, $f_o + 1\text{kHz}$
 -170dBc/Hz, $f_o + 10\text{kHz}$

phase noise at lock dependent on reference input

Jitter:

<1ps

Temperature:

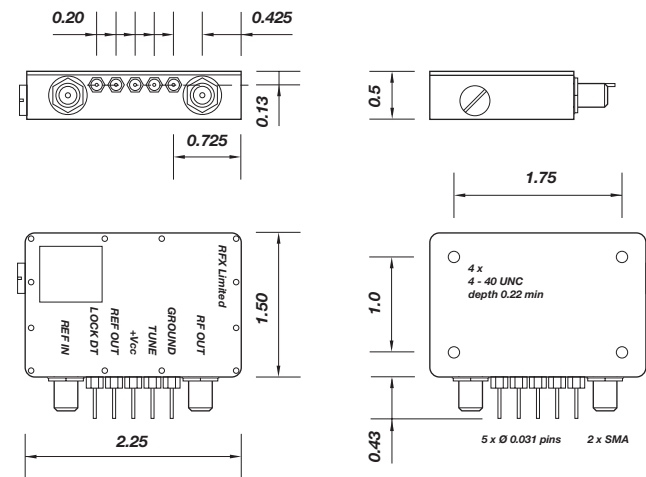
operating range (0 +50)°C
 storage range (-40 +125)°C

Insulation resistance: 500MΩ min., 100Vd.c.

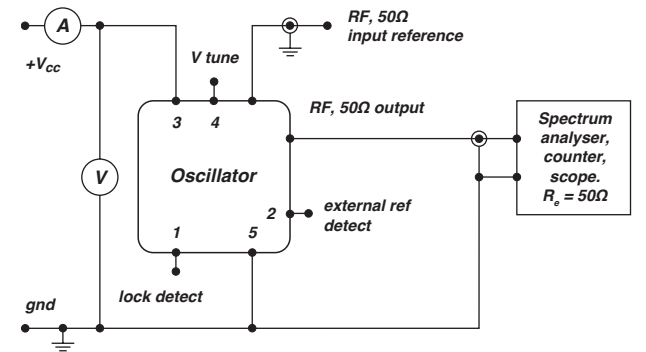
Marking:

part number, frequency, date code, serial number

Dimensions(inches):



Test circuit:



Lock detect levels:
 CMOS: low; no lock, high; lock

External ref detect levels:
 CMOS: low; no reference, high; ref detected